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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,154	07/11/2000	Martin J. Edwards	PHB 34,365	1602

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2673	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/614,154	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 1899*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of independent claim 9: "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a. respective bus line, wherein a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The limitation of independent claim 9: "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a. respective bus line, wherein a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" is not described in the disclosure.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how limitation of claim 9 "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a. respective bus line, wherein a first address conductor of a first group of address

conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" could be implemented since Figures 4-5 disclose signals processing circuits 1 and 9 adjacent to each other and at the one border of the same group. It is not clear, how the main objective of the invention could be achieved, since in claim 9 those processing circuits still far apart on the substrate opposite to what is stated in the disclosure (See page 4, Lines 16-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. US Patent No. 6, 166, 715) in view of Ohwada et al. (US Patent No. 5,021,774).

As to claim 9, as best understood by examiner, Chang et al. teaches an active matrix array device (See Col. 1, Lines 6-11) comprising:

a substrate (See Fig. 2, items 200-260, Col. 2, lines 20-29);

an array of individually addressable matrix elements carried on substrate (See Fig. 2, item 200);

a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 4, items PIX 1- PIX 40), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 4, items PIX 1- PIX 640, Col. 5, Lines 18-49);

and an addressing circuit including

a multiplexing circuit (See Fig. 4, items EN1-EN16) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (See Fig. 4, items PIX 1- PIX 640, Col. 5, Lines 18-49),

and a plurality of signal processing circuits (See Fig. 3, Items 245 (1)-245 (40)) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 3, items Y1-Y40, from Col. 3, Line 26 to col. 4, Line 3).

Matsueda et al. does not show a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate.

Ohwada et al. teaches a first signal processing circuit (See Fig. 7, items 11, Φ2) associated with a first address conductor of a first group of address conductor (See Fig. 7, item 11) and a second signal processing circuit associated with a last address

conductor of a second group of address conductors (See Fig. 7, items 11, Φ1) are adjacent on substrate (See Col. 9, Lines 53-63 and Col. 6, Lines 53-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching Ohwada et al. into the Chang et al. system in order to provide a high-speed scanning method and circuit (See Col. 3, Lines 11-14 in the Ohwada et al. reference).

As to claim 10, Chang et al. teaches signal processing circuits are arranged in series in a line parallel to multiplexing circuit (See Fig. 2-4, items 240, 260, Col. 3, Lines 26-47 and Col. 5, Lines 17-47).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. and Ohwada et al. as applied to claim 9 above, and further in view of Matsueda et al. (US Patent 6, 384, 806).

Chang et al. and Ohwada et al. do not show an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected.

Matsueda et al. teaches an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Matsueda et al. into Chang et al. and Ohwada et al. system in order to simplify circuit arrangement (See Col. 1, Lines 59-67).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohwada et al. in view of Matsueda et al.

Ohwada et al. teaches an active matrix array device (See Col. 1, Lines 9-14) comprising:

a substrate (See Fig. 1, item 16, Col. 6, lines 53-63);

an array of individually addressable matrix elements carried on substrate (See Fig. 1, item 18);

a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 1, item 12), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 1, items Φ1-Φ3, Col. 7, Lines 9-27);

and an addressing circuit including

a multiplexing circuit (See Fig. 1, item 3) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (See Fig. 1, items Φ1-Φ3, Col. 7, Lines 9-27),

and a plurality of signal processing circuits (See Fig. 1, item 11) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 1, items 11-12, from Col. 6, Line 53 to Col. 7, Line 27).

Ohwada et al. does not show an order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected.

Matsueda et al. teaches an order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, Col.20, Lines 29-45). Notice that processing circuit blocks (D/A converters and other in the reference) are located on both sides of LCD panel.

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Matsueda et al. into Chang et al. system in order to simplify circuit arrangement (see Col. 1, Lines 59-67).

Response to Arguments

7. Applicant's arguments filed on 01-24-05 with respect to claim 9-13 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS

05.12.05

VIJAY SHANKAR
PRIMARY EXAMINER